Adaptive Digital Power Systems Using Mean-Square Algorithms

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The energy industry is fundamental in that it powers every other modern industry. As engineers, we often take for granted how our energy sources are developed, maintained, and improved upon since power is typically a secondary resource used to achieve a primary objective. But from the end user perspective, energy serves the role of a force multiplier. It is a means of amplifying our well-being as we travel through everyday life, in search of cheap, reliable, and robust means of electrification. From an enterprise perspective, where access to the grid is trivial, novel solutions in power electronics are often unnecessary. But to those who operate in the off-grid portable space, any means of optimizing efficiency, or maximizing power density is cause for canine-like salivation. To the extent that we can improve our portable energy solutions, we stand to gain immense operational results in how we consider and measure product performance. It is to this end that we seek to investigate seemingly niche solutions in the problem area of autonomous and optimal power design.

Researchers in this field tend to focus their efforts on control-, device-, and system-level perspectives as highlighted in Fig. 1. For the purposes of this article, we will concentrate on the control domain, with emphasis on how digitization improves performance. The following sections will discuss the advantage of digital control in advanced communication systems, leading research methods for achieving adaptive control, and a test-bed for experimenting, comparing, and validating digital control methods.

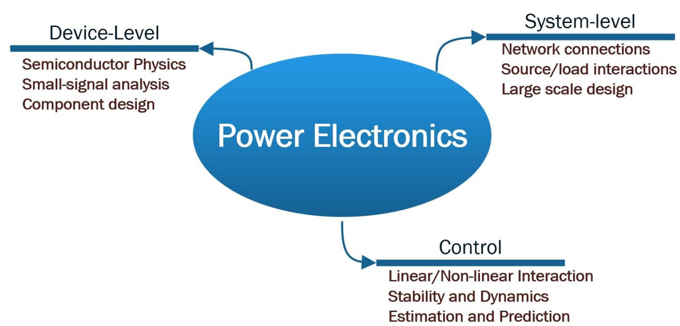

Figure 1: Common Research Areas in the of Study of Power Electronics.

Digital Power in Communications

In the radio communications space, digitization has led to the wide-spread adoption of Software-Defined Radio (SDR) technology. SDR is essentially a method to utilize a programmable digital system to establish a more flexible RF system. The approach is typically achieved using Field Programmable Gate Arrays (FPGA) as the means of achieving flexible, stable and configurable computation. But if we put our energy "hat" on for a moment, and think about our RF system not in terms of radio fundamentals, but simply in terms of energy, we are captivated by one key metric; efficiency. To the extent that we maximize efficiency, we optimize our battery life, and ultimately the operational time of the system. From this child-like view of the RF world we simply ask the question; which parts of the system use the most power? We then focus our efforts on maximizing the design efficiency at the locations identified.

This brings us to the infamous RF power amplifier (PA). In the gauntlet of communications, this is the last component of the RF transmitter that converts low power RF signals into higher power waveforms expected at the system antenna port. It is here that the majority of the system DC power is consumed and thus where the main battle for efficiency shall be fought. The power electronics circuit for this section is referred to as the *drain*

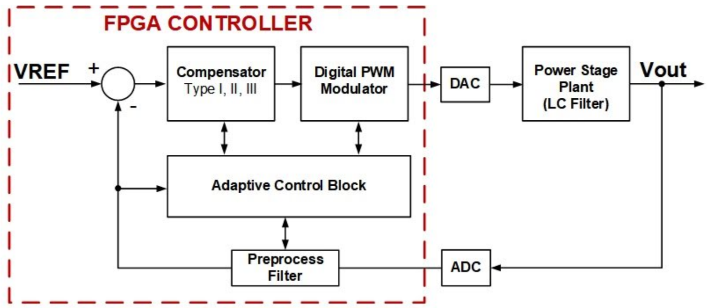

Figure 2: Block Diagram for an Adaptive Digital Control System.

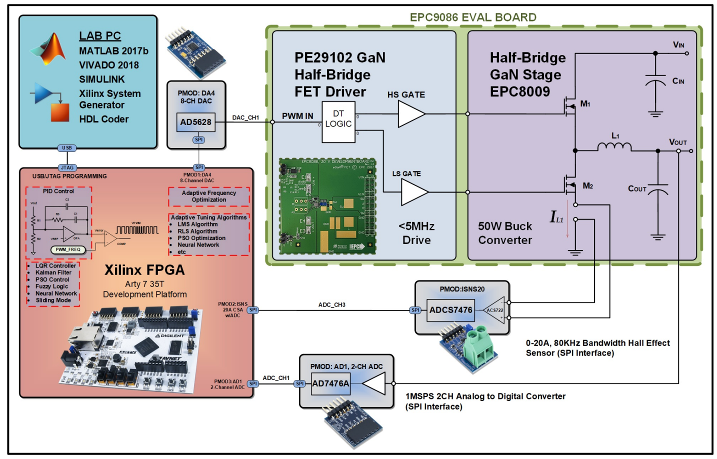

Figure 3: Experimental Test Setup for Evaluating Digital Control Solutions via FPGA.

supply since its output must be configured to match the modulated RF signals peak bias level. For radio platforms that operate in various presets and modes (UHF, VHF, MANET, SATCOM, etc), the *drain supply* must be adjusted to meet the different power requirements of the specified RF mode. This requires the circuit to operate across a wide range of output voltages, typically between 5V and 60V. If we consider that most RF systems also operate from a battery source (7V-34V), then we have a circuit that must maintain stable operation over a widely varying operating envelope. The implication is that digital control offers us advantage and opportunity to adaptively tune and optimize dynamic performance as external conditions change such as; preset mode, input level, and source/load interactions. Thus, the realization of an adaptive digital power supply enables further techniques for maximizing efficiency.

An FPGA Based Control System

So far the case has been made for adaptive digital control, but how best can we implement this in the real world? The standard approach is to utilize a microprocessor due to ease of use and cost advantages. This is perfectly valid for most use-cases but in systems that require more configurability, parallel processing, and face real-time latency challenges, FPGA based control has distinct advantages.

The control system components necessary to realize a digital power supply are shown in Fig. 2. Highlighted in red are the algorithms and functions implemented by the FPGA, resulting in closed-loop control. First, the output voltage is measured and preprocessed to filter noise. This generates a reduced power signal for the adaptive control block that is compared against an arbitrary reference signal for setting the output voltage. The adaptive control block implements a regression algorithm to tune compensator coefficient variables that result in optimum transient performance. For a full discussion on the development of a digital compensator, please see [1]. We begin from the well known form of the discrete-time transfer function for a 2-pole, 2-zero controller;

$$G_s = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}. \quad (1)$$

From this equation, we are interested in tuning the values of the a_n and b_n coefficients to achieve optimum dynamic response. Astute signal processing engineers will recognize this form as the common infinite impulse response (IIR) filtering structure. The use of digital filter performance to control impulse response has been widely studied for performance feedback since its development in the 1960s [2]. When an input signal flows into the filter, the output error signal is used to estimate the mean squared error, and then the coefficients of the filter are adjusted to minimize that error. Thus, the filter converges to the optimal impulse response. When this simple learning process is applied to a power electronics compensator, the self-optimizing filter provides optimal transient dynamics in response to both internal and external circuit conditions. When we refer to dynamics, we simply imply the best possible circuit physics including; output voltage overshoot, undershoot, slew-rate, stability, and settling time [3]. Our interest is to compare and contrast a variety of competing control algorithms for application in digital power electronics as shown in Table 1.

Algorithms	**MSE**	**Stability**	**Complexity**
LMS	0.01	$2N+1$	Less Stable
NLMS	0.009	$3N+1$	Stable
RLS	0.007	$4N^2$	More Stable
APA	0.005	$3N+1$	Most Stable

Table 1: Comparison of Adaptive Algorithms

The Path Forward

The design approach of using an FPGA based controller is justified by its long history as an adaptive signal processing solution. It allows for the rapid reconfigurability of comparing different filtering algorithms, while achieving best-in-class latency performance for real-time high-bandwidth power design. Furthermore, since SDR technology already relies on FPGA resources for RF processing, a low-utilization DC power control scheme can be realized from existing system components. Communication systems with power electronics that operate under strict performance criteria stand to benefit greatly from digital control. Adaptive digital compensators allow for power stages to be rapidly actuated which enables improvements in overall efficiency. This is why we will continue to investigate novel adaptations of existing filtering algorithms for use with different power stage circuit designs. Future work will be to develop a fully adaptive *drain supply* that adjusts its transient behavior autonomously in response to both internal and external circuit conditions.

References

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